REMARKS

The Office Action dated September 8, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-15 are presently pending in the subject application. Claims 1-15 are respectfully submitted for consideration.

Claims 1-15 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,760,341 (*Erimli et al.*). The Office Action took the position that *Erimli* taught each and every element of the claims. Applicants respectfully traverse.

Claim 1, upon which claims 2-4 are dependent, recites a network of switches. The network includes a first switch having a first memory interface and a first expansion port. The network also includes an expansion bus having a first expansion bus interface and a second expansion bus interface. The first expansion bus interface is connected to the first expansion port. The network of switches also includes a second switch having a second memory interface and a second expansion port. The second expansion port is connected to the second expansion bus interface, thereby connecting the first switch to the second switch. The expansion bus allows the first switch to directly access the second memory interface through the second switch and the second switch to directly access the first memory interface through the first switch.

Claim 5, upon which claims 6-8 are dependent, recites a switch for transmitting and receiving data packets. The switch includes a memory interface that accesses memory. The switch also includes an expansion port connected to the memory interface.

The expansion port is configured to be connected to an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory.

Claim 9, upon which claims 10-12 are dependent, recites a system of network switches. The system includes a first switch having a first memory and a first expansion port. The system also includes an expansion bus having a first expansion bus end and a second expansion bus end. The first expansion bus end is connected to the first expansion port. The system also includes a second switch having a second memory and a second expansion port. The second expansion port is connected to the second expansion bus end, thereby connecting the first switch to the second switch. The expansion bus allows the first switch to directly access the second memory through the second switch and the second switch to directly access the first memory through the first switch.

Claim 13, upon which claims 14 and 15 are dependent, recites a method for sharing memory between a first switch and a second switch connected to each other by an expansion bus. The method includes sending a command from a first switch to a second switch that the first switch is about to perform a memory read or write. The method also includes reading or writing a portion of packet data to local memory of the first switch. The method also includes reading or writing another portion of packet data to alternate memory through the second switch using the expansion bus.

As discussed in the specification, examples of the present invention provide a switch having virtual shared memory. Examples of the present invention enable an expansion port to be provided on a switch to connect two switches together. Thus, two

switches may read and write 128 bits at a time while maintaining a single memory bus master for each memory to reduce memory bus loading. Further, examples of the present invention may eliminate the need for two switches to be electrically connected to a centralized memory along a common bus. Thus, an electrical load may be decreased as compared to the use of a common bus. It is respectfully submitted that the cited reference fails to disclose or suggest all the elements of any of the presently pending claims. Therefore, the cited reference fails to provide the critical and unobvious advantages discussed above.

Erimli relates to the segmentation of buffer memories for shared frame data storage among multiple network switch modules. *Erimli* describes a network switching system with a plurality of multiport switch modules and connected buffer memory devices that assign, in each of the buffer memory devices, a memory segment for storage of frame data using a corresponding one of the switch modules. Each memory device is divided into memory segments, such that each memory segment is configured for storing frame data from a corresponding one of the switch modules. Switching logic 28 of *Erimli* forwards a frame pointer specifying the location of the received data packet to the other multiport switches 22 via an expansion port 30. Network switch port 22 receives data packet 22a and stores the received data frame in each of the buffer memory devices 36 at the same prescribed location within memory segment 40 assigned to the corresponding switch module 22. Each of switch modules 22 include a memory interface 44 configured for controlling the storage of frame data in buffer memory devices 36

according to a prescribed protocol. Memory interfaces 44 assign memory segment A in each of buffer memory devices 36 to switching module 22a, memory segment B in each of buffer memory devices 36 to switching module 22b, and memory segment C in each of the buffer memory devices 36 to switching module 22c. Thus, switch module 22a can write frame data only into memory segment A of buffer memory devices 36a, 36b and 36c and so on. Each memory interface 44 can use a single frame pointer that specifies a specific memory address location and read frame data for a stored data frame from memory devices 36. Multiple transfers may occur between memory interfaces 44a, 44b and 44c according to a prescribed cascaded sequence to optimize bandwidth on data bus 38. *Erimli*, however, does not disclose or suggest the feature of an expansion bus allowing the first switch to directly access the second memory interface through the second switch and the second switch to directly access the first memory interface through the first switch.

In contrast, claim 1 recites "said expansion bus allows said first switch to directly access said second memory interface through said second switch and said second switch to directly access said first memory interface through said first switch." Claim 5 recites "an expansion port connected to said memory interface, wherein said expansion port is configured to be connected to an expansion bus connected to another switch, thereby connecting two switches together allowing for sharing of memory." Claim 9 recites some features similar to claim 1, but is directed to a system of network switches. Claim 13 recites "reading and writing another portion of packet data to alternate memory through

said second switch using said expansion bus." Applicants respectfully submit that *Erimli* does not disclose or suggest at least these features of the claims.

Applicants submit that the cited reference does not disclose or suggest using an expansion bus to directly access a second memory interface from a first switch or a first memory interface from a second switch. *Erimli* describes storing segments of data frames in specific predetermined locations in separate switches. As noted above, the segments may be saved to the memories in a cascaded format between a plurality of switches. *Erimli* does not disclose or suggest directly accessing these memories from one switch to another through an expansion bus. For example, *Erimli* does not disclose or suggest switching module 22a of Figure 2 directly accessing memory interface 44c. Further, *Erimli* does not disclose or suggest bus 32 of Figure 2 providing access to any memory interface of the switching modules.

Further, *Erimli* does not disclose or suggest an expansion bus connecting two switches together to allow for the sharing of memory. Instead, in *Erimli*, memory devices are divided into memory segments to store frame data indicated by a frame pointer specified by a switching logic. These aspects of *Erimli* do not disclose or suggest an expansion bus that allows a first switch to directly access a second memory through a second switch and a second switch to directly access a first memory through the first switch. Thus, for at least these reasons, applicants submit that *Erimli* does not disclose or suggest at least these features of the presently pending claims.

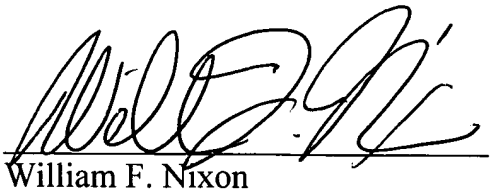
In addition, the dependent claims are allowable because of their dependency on independent claims 1, 5, 9 and 13 and because they recite subject matter in addition to independent claims 1, 5, 9 and 13. Applicants submit that the dependent claims recite subject matter that is not disclosed or suggested by *Erimli*. Therefore, each of claims 1-15 are not anticipated by *Erimli*. Applicants respectfully request that the anticipation rejection be withdrawn.

In conclusion, it is further submitted that each of claims 1-15 recites subject matter that is neither disclosed nor suggested by the cited reference. It is therefore respectfully requested that all of claims 1-15 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



William F. Nixon
Registration No. 44,262

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

WFN:cct/mm